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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Takumi HASEGAWA

Appln. No.: 09/273,560 Group Art Unit: 2682

Confirmation No.: unknown Examiner: D. To

Filed: March 22, 1999

For: DELAY ANALYSIS SYSTEM

AMENDMENT UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated October 12, 2001 please amend the above-identified application as follows (being that January 12, 2002 is a Saturday, our response date for filing is January 14, 2002):

IN THE SPECIFICATION:

Please enter the following changes to the specification:

On page 6, replace the paragraph beginning "The table shown..." at line 4 with:

A1

"The table shown in FIG. 1(b) represents delay times for the combinations of an input pin and an output pin as they rise or fall. For example, on the first line, the delay time of 1 ns means that the delay between the time the signal at the input pin (terminal 1) of a 2-input AND element goes from low to high (rises) and the time the signal at the output pin (terminal 3) goes from low to high (rises) is 1 ns. Similarly, on the fifth line, the delay time of 5 ns means that the delay